## AMENDMENTS TO THE SPECIFICATION:

**Please amend the paragraph on page 6, lines 24-25, as follows:**

Figs. 9A, 9B and 9C ~~are diagrams useful in describing setting of toggle rate and transition probability of an array~~ illustrate an example of implementation of an array variable, shown in Fig. 9A as an array *c* in the clock-based description, to be either a gate-level flip-flop register array, exemplarily shown in Fig. 9B, or a memory, exemplarily shown in Fig. 9C ;